REMARKS

Summary of the Office Action

Claims 1-4, 15-18, and 29-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seltzer et al. U.S. Patent No. 4,833,651 ("Seltzer") in view of Williams et al. U.S. Patent No. 5,084,841 ("Williams").

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Seltzer in view of Williams and further in view of M. M. Mano, Computer System Architecture, Prentice-Hall, Inc., pp. 97-98, 1976 ("Mano").

Claims 6-14 and 33-35 were objected to as being dependent upon a rejected based claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19-28 were allowed.

Summary of Applicants' Reply

Applicants note with appreciation the allowance of claims 19-28 and the indication of allowable subject matter in claims 6-14 and 33-35.

Claims 6-14 and 33-35 were objected to as being dependent upon a rejected based claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This has been done as follows:

Applicants have proposed amending claim 1 to include the features of dependent claims 5 and 6, which have been proposed to be canceled.

Applicants have proposed amending claim 29 to include a feature of dependent claim 35.

Applicants have also proposed amending claims 22 and 26 to correct typographical errors.

Applicants respectfully submit that the proposed claim amendments, if entered, moot the rejections under 35 U.S.C. § 103(a).

Reply to Rejections Under 35 U.S.C. § 103(a)

Applicants respectfully submit that the combination of Seltzer and Williams fails to render obvious the claimed invention.

If amended as proposed, claims 1 and 29 distinguish over the combination of Seltzer and Williams by describing a Gray code circuitry that is based on a "double-increment Gray code" (present application, claim 29). Neither Seltzer nor Williams describes, teaches, or suggests a shift-register-based FIFO implementation using a double-increment Gray code counter circuitry.

Both Seltzer and Williams are directed at RAM-based FIFO memories that have dedicated RAM devices with FIFO characteristics. In contrast, the present invention is directed to a FIFO memory implementation in a programmable logic device "PLD" using 5 simple circuit components (present application, FIG. 1), including shift register circuitry 60 shown in FIGS. 1 and 5 that shifts data words in accordance with Gray code values output by Gray code counter circuitries.

There is no suggestion or motivation in Seltzer that its FIFO memory should be implemented with the simple design of the present invention using a double-increment Gray code counter (counter 30 shown in FIG. 1 of the present application) and a shift register circuitry (shift register 40 shown in FIG. 1 of the present application) that "is effectively a subtractor operating on Gray code or Gray-code inputs" (specification, p. 13, lines 31-32). In fact, Seltzer teaches away from a simple PLD implementation of a FIFO memory using Gray code counters and a shift register subtractor circuitry by implementing its FIFO memory with a dedicated RAM having a write pointer, a read pointer, and a control input in addition to the write output, read input and clock signals.

The write pointer and read pointer shown in Seltzer FIG. 1 "are synchronous binary incrementing counters" (Seltzer, col. 6, lines 6-7) that are used as

inputs to the RAM itself. The Gray code counters of the present invention are only used as inputs to the shift register subtractor circuit (circuit 40 shown in FIG. 1 of the instant application) and not as inputs to the shift register circuitry used for storing data words (circuit 60 shown in FIG. 1 of the instant application).

The Examiner has suggested that replacing the binary counters of Seltzer with the Gray code counters in Williams would render obvious the present invention. Applicants respectfully disagree. Like in Seltzer, there is no suggestion in Williams that FIFO 12 (Williams, FIG. 1A) should be implemented with "shift register circuitry shifting in write data words in synchronism with the write clock signal" (present application, claim 1) based on a control input from a Gray code subtractor circuit (circuit 40, shown in FIG. 1 of the present application).

The Gray code counters disclosed in Williams are part of "status generating circuit 14" (Williams, FIGs. 1A-B) and are used to "generate Full, Half-Full, Empty, Full - N, and Empty + N status flags" (Williams, col. 3, lines 10-11). None of the Gray code counters disclosed in Williams is based on a "double-increment" (present application, claim 29) Gray code.

The lack of means for providing a FIFO memory that is implemented with "shift register circuitry shifting in write data words in synchronism with the write clock signal" (present application, claim 1) based on a control input from a Gray code subtractor circuit (circuit 40, shown in FIG. 1 of the present application) in any of the prior art references is a strong indication that those means were not obvious at the time the invention was made.

Therefore, because there is neither suggestion nor motivation to combine Seltzer and Williams and because the combination of Seltzer and Williams fails to disclose all the limitations of claims 1-35, if amended as proposed, applicants respectfully submit that the existing rejections have been obviated by the proposed amendment and that

proposed amended claims 1-35 distinguish from, and are allowable over, the cited references.

Conclusion

Applicants respectfully submit that claims 1-35, if amended as proposed, would be in condition for allowance. Reconsideration, entry of the proposed amendments, and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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